DETAILED ACTION

This office action is in response to the filing of the Applicant Amendment on 7/14/09. A note about the Examiner-Initiated Interview is included in the Response to Arguments below.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features of claims 6 and 10 must be shown or the feature(s) canceled from the claim(s). For instance, none of the figures show features of claim 6 including gate lines being arranged on the gate insulation film; data lines being arranged on the interlayer insulation layer; a passivation film arranged on the data lines. Also, none of the figures show features of claim 10 including gate lines and data lines arranged on the first insulation film; and a second insulation film arranged on the gate lines and the data lines. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

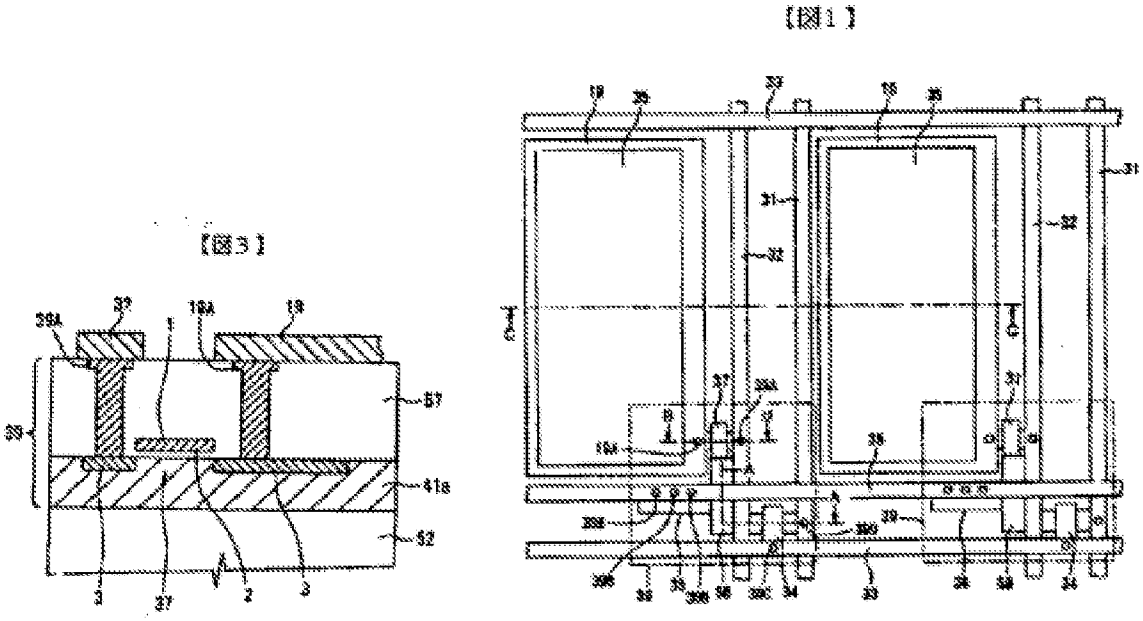
> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. **Claims 1 and 3** are rejected under 35 U.S.C. 102(b) as being anticipated by Nozawa et al. (JP 2003-15548).

4. **In re claim 1**, Nozawa et al. shows a flat panel display, comprising (Figure 3):

- a gate line 33, a data line 31 and a power supply line 32 arranged on an insulation substrate 52;
- a pixel region defined by the gate line 33, the data line 31 and the power supply line 32 (also Figure 1);
- and a pixel comprising a pixel electrode 19 arranged in the pixel region, the pixel electrode 19 being arranged on the same layer as the power supply line 32, wherein the power supply line 32 is arranged on a layer different from the gate line 33, and wherein the power supply line is arranged on a layer different from the data line 31. In the instant case, the power supply line 32 is not arranged on data line 31. The power supply line 32 is also not arranged on the gate line 33.



5. **In re claim 3**, Nozawa et al. teaches that the power supply line 32 and pixel electrode 19 both being comprised of the same material (Figure 3).

6. **Claims 1 and 10 – 13** are rejected under 35 U.S.C. 102(e) as being anticipated by Noguchi et al. (US Patent 6,762,564).

7. **In re claim 1**, Noguchi et al. shows a flat panel display, comprising (Figures 2 and 3, below):

- a gate line SL/18b/18a, a data line DL/24a and a power supply line Vdd arranged on an insulation substrate 10;
- a pixel region defined by the gate line SL, the data line DL and the power supply line Vdd;

- and a pixel comprising a pixel electrode 28 arranged in the pixel region, the pixel electrode 28 being arranged on the same layer 26 as the power supply line Vdd, wherein the power supply line Vdd is arranged on a layer different from the gate line SL/18a/18b, and wherein the power supply line Vdd is arranged on a layer different from the data line DL/24a.

8. **In re claim 10**, Noguchi et al. teaches a flat panel display, comprising (Figures 2 and 3):

- an insulation substrate 10 divided into a plurality of pixel regions, each of said pixel regions being defined by a crossing of a gate line SL (or 18a) and a data line DL (or 24a), the insulation substrate 10 comprising a plurality of thin film transistors Tr1/Tr2, each thin film transistor being arranged in corresponding ones of said plurality of pixel regions;
- a first insulation film 16 arranged on the substrate 10 and on the plurality of thin film transistors Tr1/Tr2;
- a gate electrode 18a, gate lines SL and data lines DL (or 24a) arranged on the first insulation film 16;
- a second insulation film 26 arranged on the gate electrode 18a, the gate lines SL and the data lines DL;
- a plurality of pixel electrodes 28 arranged on the second insulation film 26 and being electrically connected to corresponding ones of said plurality of thin film transistors Tr2 in corresponding ones of said plurality of pixel regions; and

- a power supply layer Vdd also arranged on the second insulation film 26, the power supply Vdd layer being electrically separated from the plurality of pixel electrodes 28, said power supply layer Vdd being electrically connected to each of the plurality of thin film transistors Tr2 and supplying power to each of the plurality of thin film transistors Tr2.

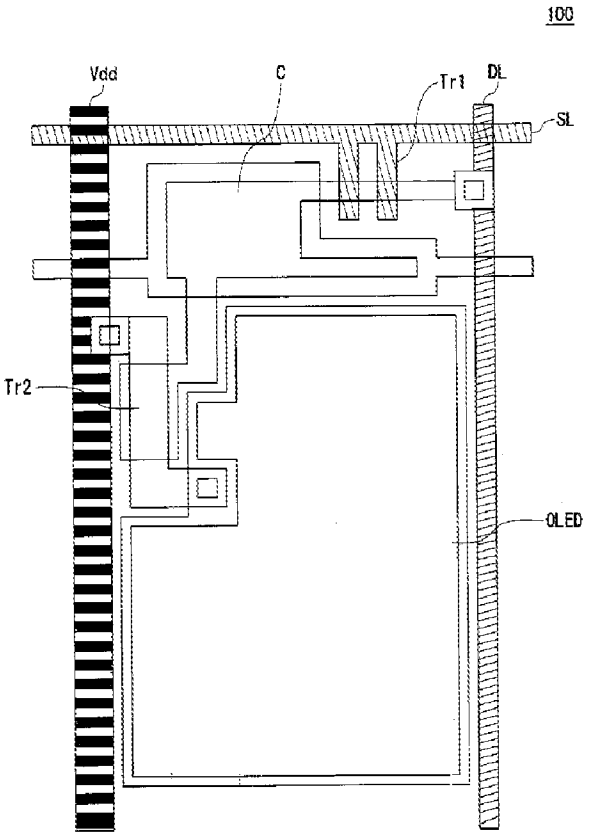

100
Vdd
C
Tr1
DL
SL
Tr2
OLED

FIG. 2

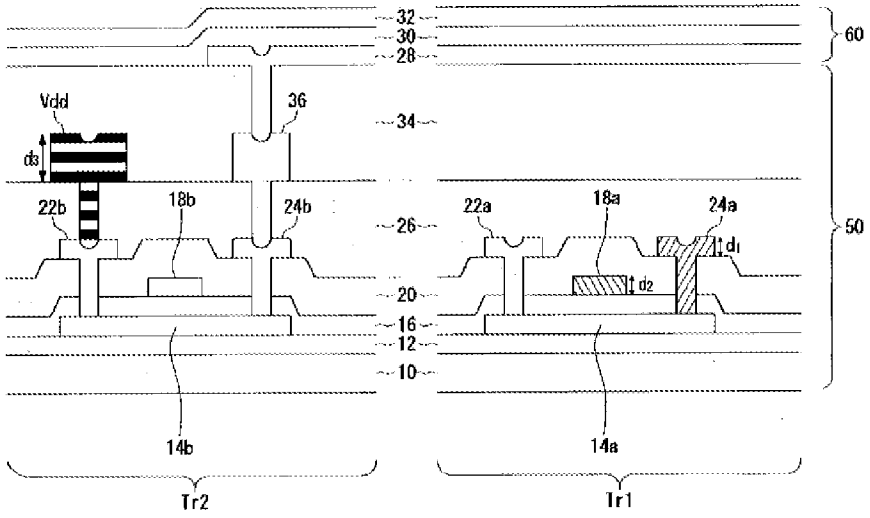

32
30
28
60
Vdd
36
34
ds
22b
18b
24b
26
22a
18a
24a
d1
d2
50
20
16
12
10
14b
14a
Tr2
Tr1

FIG. 3

9. **In re claim 11**, Noguchi et al. shows that an entirety of the power supply layer Vdd is separated from an entirety of each of the gate lines SL (and 18a) and the data lines DL (also 24a) by the second insulation film 26 (Figure 3).

10. **In re claim 12**, Noguchi et al. shows that the power supply layer Vdd being formed in a line shape in which the power supply layer Vdd is arranged between corresponding ones of said plurality of pixel electrodes 28 of OLED, said power supply layer Vdd being arranged in one of a row or a column (Figure 2, also implied by Column 1, Line 8 – 9 and Column 2, Line 37 - 38).

11. **In re claim 13**, Noguchi et al. shows that the power supply layer Vdd having a surface electrode shape in which the power supply layer Vdd is formed on a whole surface of the substrate 10 and being electrically separated from each of the plurality of pixel electrodes 28 (Figure 3).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. **Claims 4 – 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozawa et al. in view of Koyama (US PGPub 2003/0117083). Nozawa et al. does not teach that pixel electrode 19 is made from a material meeting the claimed characteristics, however, Koyama et al. teaches that electrode 49 can be gold (Figure

4). It would have been obvious to one having ordinary skill in the art at the time of the invention to use gold for a pixel electrode since doing so would allow for one to make a top emitting device such as shown by Koyama. Also, Nozawa et al. teaches that power supply line 32 is made from a conductive material such as metal (Paragraph 61). Koyama et al. teaches that gold is a conductive metal. It would have been obvious to one having ordinary skill in the art at the time of the invention to use gold for the power supply line of Nozawa et al. since Nozawa et al. suggests using a conductive metal and it is well known that gold is a very good conductor. This combination would teach that both the pixel electrode and power supply line be made of gold. Gold has low resistivity and high reflectivity.

14. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi et al. in view of Komiya et al. (US Patent 6,724,149). Noguchi et al. does not teach that the power supply layer has a grid shape and surrounds a pixel region, however, Komiya et al. teaches that power supply layer 181 & 183 surrounds a pixel region 160. It would have been obvious to one having ordinary skill in the art at the time of the invention to make the power supply layer of Noguchi et al. into a grid pattern since doing so enhances the uniformity of luminescence from the pixel region (Komiya et al., Column 8, Lines 55 – 67).

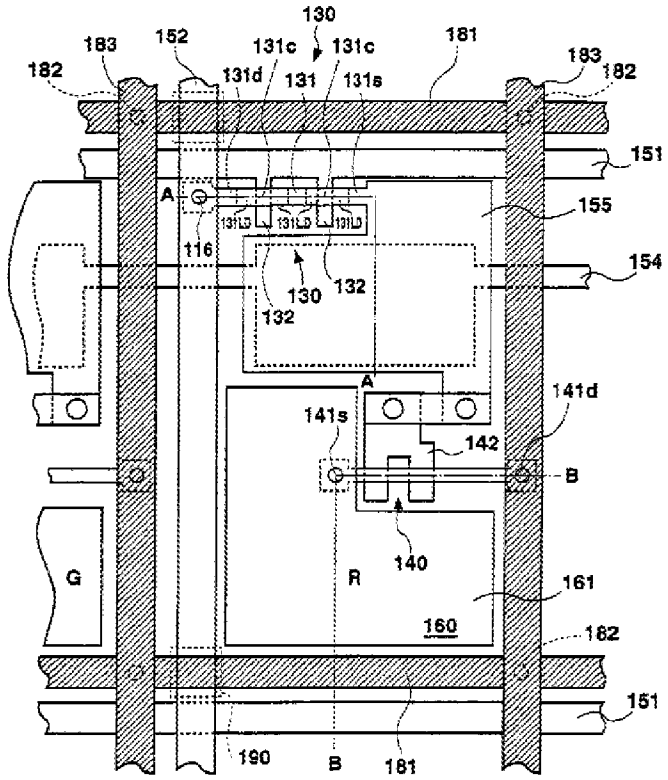


Fig. 4

15. **Claims 6 – 9 and 21 – 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi et al. in view of Koo et al. (US PGPub 2003/0111954).

16. **In re claim 6**, Noguchi et al. teaches a flat panel display, comprising (Figures 2 and 3):

- a thin film transistor Tr2 comprising source and drain electrodes, formed arranged on an insulation substrate 10;
- a gate insulation film 16 arranged on the insulation substrate 10 and on the thin film transistor Tr2, the gate insulation film 16 being perforated by first and

second contact holes (filled with 22b & 24b) exposing the source and drain electrodes respectively;

- a gate electrode 18b and gate lines SL being arranged on the gate insulation film 16;
- an interlayer insulation film 20 arranged on the gate electrode 18b and the gate lines SL;
- data lines DL (also 24a) being arranged on the interlayer insulation film 20;
- a passivation film 26 arranged on the data lines DL (also 24a);
- a pixel electrode 36 arranged on the passivation film 26 and electrically connected to one of the source and drain electrodes through one of the first and second contact holes 24b; and
- a power supply layer Vdd also arranged on the passivation film 26 and electrically connected to the other one of the source and drain electrodes through the other one of the first and second contact holes 22b.

Noguchi et al. does not disclose that the lower electrode of a capacitor is arranged on the gate insulation film. Noguchi et al. also does not disclose that the upper electrode of the capacitor is on the interlayer insulation film. Noguchi et al. teaches a capacitor (Column 3, Line 10 – 15). Koo et al. teaches that a first electrode of a capacitor is directly on the same gate insulating layer as is the gate electrode and that a second electrode of the capacitor is directly on the same insulating layer as is the data line (Paragraphs 7 and 11). It would have been obvious to one having ordinary skill in the art a the time of the invention to make one of the capacitor electrodes of Noguchi et al.

on the gate insulation film 16 and make the other capacitor electrode of Noguchi et al. on the interlayer insulation film since it was well known to arrange one capacitor electrode level with the gate electrode/line and to arrange another capacitor electrode level with the data line in order to create a functioning pixel.

17. **In re claims 7 and 8**, Noguchi et al. teaches that power supply layer Vdd can be aluminum (Column 7, Line 10). Noguchi et al. does not disclose what pixel electrode 36 is, however, it would have been obvious to one having ordinary skill in the art at the time of the invention to make it aluminum since it was well known to have high conductivity. Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice (In re Leshin, 125 USPQ 416, 1960, please also see MPEP §2144.07). Aluminum has both a low resistivity and a high reflectivity.

18. **In re claim 9**, Noguchi et al. teaches that the pixel electrode 36 and the power supply layer Vdd are level, however, Noguchi et al. does not teach that they are comprised of a single film of a material. Koo et al. teaches that two electrodes 141 & 142 that are level are made of the same film (Paragraph 33). It would have been obvious to one having ordinary skill at the time of the invention to create the pixel electrode 36 and the power supply layer Vdd of a single film of a material since doing so would create the two simultaneously. Noguchi et al. does not teach any of the claimed materials, however, it would have been obvious to one having ordinary skill in the art to use gold for the pixel electrode 36 and the power supply layer Vdd of Noguchi et al. since gold has a high conductivity. Also, it has been held to be within the general skill of

a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice (In re Leshin, 125 USPQ 416, 1960, please also see MPEP §2144.07).

19. **In re claim 21**, Noguchi et al. shows that an entirety of the power supply layer Vdd is separated from an entirety of the data lines DL by the passivation film 26 (Figure 3).

20. **In re claim 22**, Noguchi et al. teaches that an entirety of the power supply layer Vdd being separated from an entirety of the gate lines SL (and also 18b) by the passivation film 26 and the interlayer insulation film 20 (Figure 3).

Response to Arguments

21. Applicant's arguments filed 7/14/09 in regards to claims 1 and 3 – 5 have been fully considered but they are not persuasive. Both Nozawa et al. and Noguchi et al. teach the claimed features. To clarify, Nozawa et al. teaches that the power supply line is arranged on a layer different from the gate line; the power supply line is not on the gate line. Also, Nozawa et al. teaches that the power supply line is arranged on a layer different from the data line; the power supply line is not on the data line.

22. Applicant's arguments with respect to independent claims 1, 6, and 10 have been considered but are moot in view of the new ground(s) of rejection.

23. Examiner *greatly appreciates* Applicant's cooperation in the proposed Examiner's Amendment as described in the attached Examiner-Initiated Interview Summary. Regretfully, reference of Noguchi et al. was found to be relevant during additional

searching. **It still stands that the cancellation of claims 1 and 3 – 5 would overcome the Nozawa et al. reference. Also, a certified translation of the foreign priority document would overcome the prior art date of the Noguchi et al. reference.**

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUN M. KIM whose telephone number is (571)270-1431. The examiner can normally be reached on Monday - Thursday 10:30 am - 8:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Landau can be reached on (571) 272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sun M Kim/
Examiner, Art Unit 2813

/W. David Coleman/
Primary Examiner, Art Unit 2823